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DAVID K LUCENTE
SEAGATE TECHNOLOGY LLC
INTELLECTUAL PROPERTY DEPT COL2LGL
389 DISC DRIVE
LONGMONT, CA 80503

EXAMINER	
NGUYEN, MIKE	
ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/494,787	MOUNT, JOHN A.
	Examiner	Art Unit
	Mike Nguyen	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-15* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *13* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Notices & Remarks

1. Claims 1-15 are pending for the examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Bowes et al. (U.S. Pat. No. 5,828,856).

4. As to claim 1, Bowes teaches in a storage system having a bus (see figure 2A element 214) operatively coupled to a first controller chip and a first channel chip (see figure 2A element 220 and figure 2B element 244 wherein the channel chip 244 is built in the controller chip 220), the channel chip having several registers (see figure 3 elements 324, 314, 322, 312, 316, 326, 366), the storage system also having a storage medium operatively coupled to the bus through a

storage medium interface (see figure 2A elements "Hard Disk Drive", 214, 228), a method for retrieving data record on a storage medium comprising the step of:

(a) retrieving a first portion of the record data via the bus (see column 5 lines 1-4 and figure 2B elements 244, 237, 214 and column 5 lines 51-54, wherein the DMA channel 244 retrieves a portion of the record data from the I/O controllers 237 via the I/O bus 214);

(b) updating some of the registers via the bus (see figure 3 elements 314, 324 and column 14 lines 31-35, wherein the I/O controller 237 couples to the multiple DMA channels via the I/O bus 214 (see figure 2B elements 237, 244, 214); therefore, updating the registers 314, 324 in the multiple DMA channels should be via the I/O bus 214.); and

(c) retrieving a second portion of the record data via the bus (see figure 2B elements 244, 214, 237 and columns 5 lines 62-65, wherein after retrieving the first portion of the recorded data in (a) and updating some registers in (b) the DMA channel 244 will repeat the process if additional data in the bus needs to transfer).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bowes as applied to claim 1 above, and further in view of Kerry C. Glover (U.S. Pat. No. 5,829,011).

7. As to claim 2, Bowes fails to explicitly teach: the method of claim 1 in which the interface includes a read head, further comprising a step (d) of repositioning the storage medium

interface with respect to the storage medium, between retrieving steps (a) and (c). Glover; however, teaches the method in which the interface includes a read head (see figure 1 and column 4 lines 45-55), further comprising a step (d) of repositioning the storage medium interface with respect to the storage medium, between retrieving steps (a) and (c) (see column 6 lines 25-30). Given the teaching of Glover, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the interface, such as taught by Glover, in order to provide improved the method of storing and retrieving data (see column 1 lines 35-40).

8. As to claim 3, Bowes fails to explicitly teach: the method of claim 2 in which the interface has plurality of operating parameters that are modified in updating step (b). Glover; however, teaches the method in which the interface has plurality of operating parameters that are modified in updating step (b) (see column 6 lines 15-25). Given the teaching of Glover, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the interface, such as taught by Glover, in order to provide eliminated of additional or dedicated serial ports, improved start-up or initialization times, and reduced fabrication costs due to the elimination of unneeded circuitry for the storage system (see column 3 lines 66-67 and column 4 lines 1-11).

9. As per claims 4, and 5, Bowes fails to explicitly teach: the storage system of claim 1 configured to perform the method of claim 1 in which the registers contain at least one read channel parameter value selected from the group consisting of: a precompensation value; a filter coefficient value; and a phase offset value, and at least one mode-indicative value. Glover; however, teaches the storage system configured to perform the method in which the registers

contain at least one read channel parameter value (see column 3 lines 7-9) selected from the group consisting of: a precompensation value, a filter coefficient value, and a phase offset value (see column 5 lines 1-39); and at least one mode-indicative value (see figure 2 and column 6 lines 25-30, wherein after the initialization routine is complete, data may be read from or written to the storage medium. The controller provides a signal and mode-indicative value to a read head so that the read head may be properly positioned on the storage medium). Given the teaching of Glover, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the storage system, such as taught by Glover, in order to provide eliminated of additional or dedicated serial ports, improved start-up or initialization times, and reduced fabrication costs due to the elimination of unneeded circuitry for the storage system (see column 3 lines 66-67 and column 4 lines 1-11).

10. Claims 6, 8-9, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bowes and Glover, and further in view of Nishida et al. (U.S. Pat. No. 5,586,098).

11. As to claim 6, Bowes teaches in a storage system having an interface configured to read data, a direct memory access (DMA) controller, a microprocessor coupled to the DMA controller (see figure 2A elements 228, 218, 222), and several read channel registers each containing a value (see column 3 lines 8-19), a method comprising steps of:

(a) retrieving via the DMA controller several values (see figure 2B element 218 and column 5 lines 51-54, wherein when the DMA controller 218 is performing a read operation, a portion of data is retrieved via the DMA controller 218 from the I/O controllers 237);

(b) updating at least some the read channel register values from the retrieved values (see

figure 3 elements 324, 314 and column 14 lines 31-35, wherein the count registers 314, 324 in the multi DMA channel 244 are updated after each transfer of data to the I/O controllers 237);

Bowes fails to explicitly teach: (c) reconfiguring the interface to read data; and reading the target segment. Glover; however, teaches reconfiguring the interface to read data (see figure 1 and column 6 lines 37-40, wherein the read/write head interface of disk/head assembly is configured to read data); and reading the target segment (see column 6 lines 40-42, wherein reading the target segment should be processed after the interface is configured to read data). Given the teaching of Glover, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the storage system, such as taught by Glover, in order to provide improved the method of storing and retrieving data (see column 1 lines 35-40);

The combination of Bowes and Glover fails to explicitly teach: in a storage system having a disc with at least two zones having zone identifiers Z_A and Z_B, a value table indexed by zone identifiers. Nishida; however, teaches in a storage system having a disc with at least two zone (see figure 5 and column 4 lines 57-59) having zone identifiers Z_A and Z_B, and a value table indexed by zone identifiers (see column 7 lines 30-33). Given the teaching of Nishida, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Bowes and Glover by employing the well-known or conventional feature of the method, such as taught by Nishida, in order to provide maintaining disk performance, including minimizing disk recording error rates, while more fully utilizing the storage capacity of each disk surface (see column 1 lines 45-49).

12. As to claim 8, the combination of Bowes and Nishida fails to explicitly teach the method of claim 6 in which the interface includes at least one head, in which positioning step (c) includes a step of (c1) moving the at least one head radically across the disc, the moving step (c1) beginning before retrieving step (a) is complete. Glover; however, teaches the interface includes at least one head (see figure 1 column 4 lines 45-55), in which positioning step (c) includes a step of (c1) moving the at least one head radically across the disc, the moving step (c1) beginning before retrieving step (a) is complete (see figure 1 and column 6 lines 37-42, 66-67 and column 7 lines 1-3 wherein during a read/write operation the read/write heads of disk/head assembly 12 are properly positioned beginning before retrieving step (a) is complete). Given the teaching of Glover, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Bowes and Nishida by employing the well-known or conventional feature of the interface, such as taught by Glover, in order to provide improved the method of storing and retrieving data (see column 1 lines 35-40).

13. As to claim 9, the combination of Bowes and Nishida fails to explicitly teach the method of claim 8 in which moving step (c1) begins before retrieving step (a) begins. Glover; however, teaches the method of claim 8 in which moving step (c1) begins before retrieving step (a) begins (see column 6 lines 25-30). Given the teaching of Glover, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Bowes and Nishida by employing the well-known or conventional feature of the interface, such as taught by Glover, in order to provide improved the method of storing and retrieving data (see column 1 lines 35-40).

14. As to claim 11, the combination of Bowes and Nishida fails to explicitly teach the method of claim 6 further comprising prior steps of: (e) configuring the interface to read data in zone Z_B; (f) receiving a signal from the interface; (g) deriving several values indicative of the interface's performance in zone Z_B from the received signal; and (h) storing some of the derived values in the value table each at a position associated with zone Z_B. Glover; however, teaches the method further comprising prior steps of: (e) configuring the interface to read; (f) receiving a signal from the interface (see column 6 lines 37-42); (g) deriving several values indicative of the interface's performance in zone Z_B from the received signal; and (h) storing some of the derived values in the value table each at a position associated with zone Z_B (see column 6 lines 37-42). Given the teaching of Glover, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Bowes and Nishida by employing the well-known or conventional feature of the storage system, such as taught by Glover, in order to provide improved the method of storing and retrieving data (see column 1 lines 35-40)

15. As to claim 12, Bowes teaches the method of claim 6 in which the storage system includes an integrated circuit comprising the microprocessor, and in which the retrieving step (a) comprises issuing at least one but fewer than 10 commands from the microprocessor to the DMA controller (see figure 2A elements 222 column 5 lines1-21).

16. As to claim 13, the combination of Bowes and Nishida fails to explicitly teach the method of claim 12 further comprising steps of: (j) sensing position data from servo sector via the interface; and (k) deriving a servo control signal from the sensed position data with the microprocessor during step (b). However; Glover, teaches the method further comprising steps

of: (j) sensing position data from servo sector via the interface (see figure 1 element 20 and column 5 lines 40-44 and column 6 lines 27-30); and (k) deriving a servo control signal from the sensed position data with the microprocessor during step (b) (see 5 lines 40-44). Given the teaching of Glover, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Bowes and Nishida by employing the well-known or conventional feature of the interface, such as taught by Glover, in order to provide improved the method of storing and retrieving data (see column 1 lines 35-40).

17. As to claim 14, Bowes teaches the storage system of claim 6 configured to perform the method further comprising a printer circuit board assembly including a memory containing the value table, the storage system (see figure 2A) comprising:

a master integrated circuit (IC) containing the microprocessor and the direct memory access controller, the DMA controller being operatively coupled to the memory (see figure 2A elements 222, 218, 224);

a slave IC containing the several read channel registers; and a bus coupled between the master IC and the slave IC, the bus controllable by the DMA controller to perform updating step (b) (see figure 3 elements 312, 322, 314, 324 and figure 2A element 214).

18. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bowes, and further in view of Nishida et al.

19. As to claim 15, Bowes teaches a disc drive comprising:

a disc stack comprising at least one disc (see figure 2A element "Hard Disk Drive");

an interface configured to read data from the at least one disc (see figure 2A element 214);

a first controller chip containing a microprocessor and direct memory access (DMA) controller, the DMA controller operatively coupled to memory (see figure 2A elements 220, 218, 224 and figure 2B element 257);

a first channel chip having several registers (see figure 2B element 244 and figure 3 elements 324, 314, 322, 312); and

a bus operatively coupled between the interface and the chips, the bus controllable by the DMA controller to read from the memory and to update several of the registers in response to a zone transition event (see figure 2B element 214).

Although the disc drive taught by Bowes shows substantial features of the claimed invention (discussed above), it fails to explicitly teach: a memory containing several values indexed by the zone identifier. Nishida; however, teaches a memory containing several values indexed by the zone identifier (see figure 6B and column 7 lines 30-33). Given the teaching of Nishida, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Bowes by employing the well-known or conventional feature of the disc drive, such as taught by Nishida, in order to provide maintaining disk performance, including minimizing disk recording error rates, while more fully utilizing the storage capacity of each disk surface.

20. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Bowes, Glover and Nishida as applied claim 6 above, and further in view of Asakawa et al. (U.S. Pat. No. 5,121,260)

21. As to claim 7, the combination of Bowes, Glover and Nishida fails to explicitly teach the method of claim 6 in which the target segment has a predetermined starting track number, further

comprising a step of deriving zone identifier Z_B from the predetermined starting track number before retrieving step (a). Asakawa; however, teaches the target segment has a predetermined starting track number, further comprising a step of deriving zone identifier Z_B from the predetermined starting track number before retrieving step (a) (see figure 1 and column 3 lines 54-63 wherein a zone identifier is defined to correlate with a selected track which is positioned by the disc drive read/write head). Given the teaching of Asakawa, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying the combination of Bowes, Glover and Nishida by employing the well-known or conventional feature of the storage system, such as taught by Asakawa, in order to provide maintaining disk performance, including minimizing disk recording error rates, while more fully utilizing the storage capacity of each disk surface.

Allowable Subject Matter

22. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

23. Applicant's arguments filed October, 30 2002 have been fully considered but they are not persuasive.

Response to the Applicant augments that Bowes does not teach "updating some of the registers via the bus". As indicated in figure 2B discloses the communication between channel chip 218 and I/O controller 237 via bus 214. Further (column 14 lines 31-35) indicated that the

registers 314 and 324 within the channel chip 218 store retrieved data and update after each transfer of data to I/O controller 237 via bus 214.

Conclusion

24. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) rejection.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is (703) 305-5040 or e-mail is mike.nguyen@uspto.gov. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

The appropriate fax number for the organization where this application or proceeding is assigned is (703) 746-7240.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Jeffrey Gaffin, can be reached on (703) 308-3301.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-3900.

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Mike Nguyen
Patent Examiner
Group Art Unit 2182

12/30/2002